PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

KUO et al.

Serial No.: 09/839,365

Filed: April 23, 2001

Group Art Unit: 1765

Examiner: V. Perez-Ramos

For: METHOD FOR FORMING CONTACT WINDOW

REQUEST FOR RECONSIDERATION

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This is in response to the Official Action of January 14, 2003, in connection with the above-identified application. The period for response to this Official Action has been extended to expire on May 14, 2003 by the filing herewith of a Petition for a One Month Extension of Time and payment of the required fee.

In addition, Applicants submit herewith a Notice of Appeal to provide the Examiner additional time to consider the present response which it is believed to overcome all the outstanding rejections and places the application in condition for allowance or to ensure that the application is in the best form for proceeding with an Appeal.

Applicants acknowledge with appreciation the courtesy of the interview extended the undersigned attorney by Examiner Vanessa Perez-Ramos and Supervisory Primary Examiner Benjamin Utech.

At the interview, the outstanding rejections were discussed and it was agreed at the interview that the rejection under 35 U.S.C. 112 will be withdrawn. This is reflected in the Examiner interview summary record.

More particularly, it is urged in the Official Action, in the rejection of claim 1 under 35 U.S.C. 112, first paragraph, that the limitations that the semiconductor structures are covered and a plurality of gaps, which are located between neighboring semiconductor structures, are totally filled by said coating layer, and are not filled by the overcoating

layer represent new matter not previously described in the specification. However, at the interview it was pointed out that the specification clearly defines this aspect of the invention when the specification is read in light of the Figures, especially Figures 2A, 2B and 2C.

As set forth on page 5 of Applicants' specification, with reference to Figure 2A, it is seen that the semiconductor structures 21 are overcoated with a coating layer 22 which is higher than the heights of the semiconductor structures 21. In addition, there is an overcoating layer 24 over the top of the coating layer 22. The gap referred to would be fully appreciated by one of ordinary skill in the art as the space between the two semiconductor structures and this point was fully appreciated during the interview. It was agreed that claim limitations in this regard are fully supported by the specification as would be interpreted by one of ordinary skill in the art. The specification includes the drawings. Accordingly, it is most respectfully requested that this rejection be withdrawn.

As also discussed during the interview, one feature of the present invention is to overcome the deficiencies of the prior art as shown with respect to Figure 1 because of the problems associated with filling the contact windows in the more highly integrated semiconductors. As noted at page three of Applicants' specification, no matter how, the allowable width of a contact window is strongly limited by the increased integration of semiconductor devices. Because each contact must be isolated with other contacts or semiconductor elements, there is a lower limitation of distance between each contact and other contacts or semiconductor element. Obviously, width of the contact window is limited by the specific critical dimension, and then the aspect ratio still is increased as depth of the contact window is increased. This is clearly shown by the structure of the contact window of the present invention as shown in Figure 2B and 2C, element 25. This specific point was discussed with Mr. Utech at the interview. There is no recognition of this "gap" situation with respect to the primary reference Donley et al.

The rejection of claims 1 and 3-11 under 35 U.S.C. 103(a) as being unpatentable over Donley in view of Jillie Jr. has been carefully considered but is most respectfully traversed. Applicants most respectfully submit that the presently claimed invention is unobvious since there is absolutely no suggestion to one of ordinary skill in the art of forming a coating layer over the surface of the wafer where the thickness of the coating

layer is not less than the heights of the semiconductor structures, and wherein the semiconductor structures are covered by this coating layer and the gaps are totally filled by the coating layer and then forming an overcoating layer over said coating layer. This is clearly shown in Figure 2 of the present specification. Moreover, the claim specifies that the etching rate of the overcoating layer is higher than the etching rate of the coating layer wherein the gaps are not filled by said overcoating layer and forming the contact window in both the overcoating layer and the coating layer wherein the upper part of the contact window is outwardly widened.

Applicants most respectfully submit that there is absolutely no motivation or teaching in the prior art which would lead one of ordinary skill in the art to the presently claimed invention, absent Applicants' teaching. In re Fritch, 23 USPQ 1780, 1784(Fed Cir. 1992) ("It is impermissible to engage in hindsight reconstruction of the claimed invention, using the applicant's structure as a template and selecting elements from references to fill the gaps.).

Applicants appreciate the Examiner's comments and detailed analysis of the references as set forth in the Official Action. It is appreciated that the Donley reference teaches at column 2, beginning at line 62, that reference is made to the drawing in which the fabrication of one IGFET will be described. It is further stated that it is to be understood that many IGFETs would be simultaneously formed in the same silicon wafer to produce one or more integrated circuits in that wafer. However, for convenience, only one such transistor for one such circuit is shown. However, there is no recognition at this point of the problem with increasing the integration as discussed in applications' specification, nor more importantly, Applicant's solution as set forth in the claims.

Specifically, it is urged on page 3 of the Official Action that Donley further discloses that "coating layer" (layer 14), completely covers all the structures in the wafers, whereas "overcoating layer" (layer 24) does not fill the gaps with specific reference to Figures 9 and 10. This statement is specifically traversed as it is believed not to correctly interpret the teaching as discussed at the interview. In this regard, the Examiner's attention is directed to Figures 7 and 8 of the Donley reference which shows that the layer 24 is etched to produce windows 26 and 28. As shown in Figure 9 of

Donley, this is covered with a glass layer 30 which is smooth and then the glass is etched and oxidized window as shown in Figure 11. This in no way suggests the presently claimed invention.

It is further urged in the Official Action on page 3 that it is the Examiner's position that, in the case where many structures are simultaneously formed, as disclosed by Donley, gaps would be located between the structures even if not disclosed, and, furthermore, upon the deposition of the coating layer such gaps would be completely filled by said coating layer as per Applicants' newly added limitations. As discussed a the interview, this is clearly not the case and the only basis for such interpretation is the teachings in Applicants' specification which may not be used as a teaching reference.

The teachings of the Jillie reference does not overcome the deficiencies of the Donley reference. Jillie's invention is related to a specific order of etching power. Thus, Jillie only discloses values of process parameters, which are not the key of his invention, are adjustable By carefully analyzing Jillie, Applicants find that Jillie utilizes a multiple step power reduction recipe. In other words, Jillie limits the power of each following etch process must be lower than the power of the former etch process. Please note at least refer to col. 1 lines 53-61, col. 2 lines 4-17, col. 2 lines 27-38, col. 2 lines 59-68, col.3 line 64 to col. 4 lines 12, col. 4 lines 38-56.

Clearly, Jillie claimed a method of sequentially etching a thin film with several power level, where each power level used by one etch process is lower than the power level used by the former etch process. For examples, Jillie's first embodiment uses 275 watts and 150 watts in sequence, and Jillie's second embodiment uses 275 watts, 150 watts, 100 watts and 75 watts in sequence. Clearly, Jillie does not limit the practical power used to etch. In contrast, Jillie really limits a specific order of etching power: for a series etching process, the power is reduced in sequence.

Additional, Jillie never discloses or teaches anything about the different etching rates between neighboring layers. In other words, Jillie is nothing about the main character and the issue of the claimed invention. This can be proven by using "etch" and "rate" as the key-words to thoroughly search Jillie.

Therefore, although Jillie really discloses the idea of "the variation of process parameters during semiconductor manufacturing is obvious to one skilled in the art",

Jillie still limits and claims a specific order of etching power. In other words, Jillie not only means that the values of parameters are adjustable for one skilled in the art, Jillie further means that the specific order of parameter(s) could be patentable.

Therefore, while Jillie's specific order of etching power being an allowed patent, the order or etching rate present by the claimed invention also could be patentable (the claimed invention never limits the practical etching rate of each rates). At least, the patentability of the claimed invention should not be rejected by only referring to Jillie and considering Jillie disclosing that the variation process parameters are obvious.

Accordingly, Applicants reasonably emphasize that the difference(s) between the claimed invention and Donley is (are) not disclosed or taught by Jillie. Thus, none of the pending claims is unpatentable over Donley in view of Jillie.

The further rejection of claims 13-18 and 20 as obvious over Donley in view of Jillie and further in view of Obeng has been carefully considered but is most respectfully traversed for the above reasons as Obeng does not overcome the deficiencies of the primary references as discussed above. Accordingly, it is most respectfully requested that this rejection be withdrawn.

In view of the above comments and previous amendments to the specification and claims, favorable reconsideration and allowance of all of the claims now present in the application are most respectfully requested.

Respectfully submitted,
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